AS3046 NPN Transistor Array

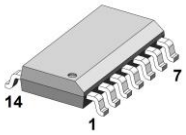
Features

- matched pair of npn transistors
- V_{BE} matched less than ±1 mV
- 5 general purpose monolithic transistors
- wide operating current range

Applications

- filters
- custom designed differential amplifiers
- temperature compensated amplifiers

AS3046D

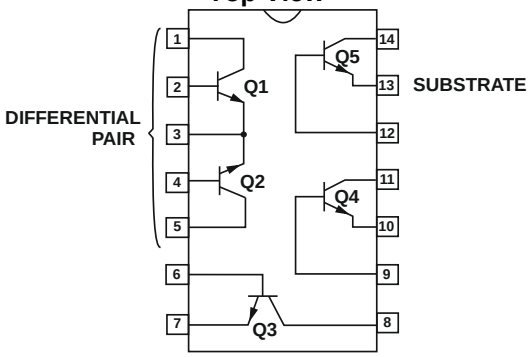


SOIC-14 150mil
1,27mm pitch

General Description

The AS3046 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The AS3046 is supplied in a 14-lead plastic SOIC-14(150Mil) package.

Connection Diagram
Top View



AS3046D
SOIC-14 (150mil)

Pin Information SOIC-14

Pin number	Description	Pin number	Description
1	Collector1	8	Collector3
2	Base1	9	Base4
3	Emitter1,2	10	Emitter4
4	Base2	11	Collector4
5	Collector2	12	Base5
6	Base3	13	Emitter5 (Substrate)
7	Emitter3	14	Collector5

Absolute Maximum Ratings	Each Transistor	Total Package	Units
Power Dissipation	200	500	mW
Collector-Emitter Voltage, U_{CEO}	30		V
Collector-Base Voltage, U_{CBO}	50		V
Collector-Substrate Voltage, U_{CIO} (Note 1)	50		V
Emitter-Base Voltage, U_{EBO}	5		V
Collector-Current, I_C	30		mA
Thermal Information			
Thermal Resistance (Typical, Note 2)	Θ_{JA} (°C/W)	Θ_{JC} (°C/W)	
SOIC Package	220	N/A	

NOTES:

1. The collector of each transistor of the AS3046 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. Θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

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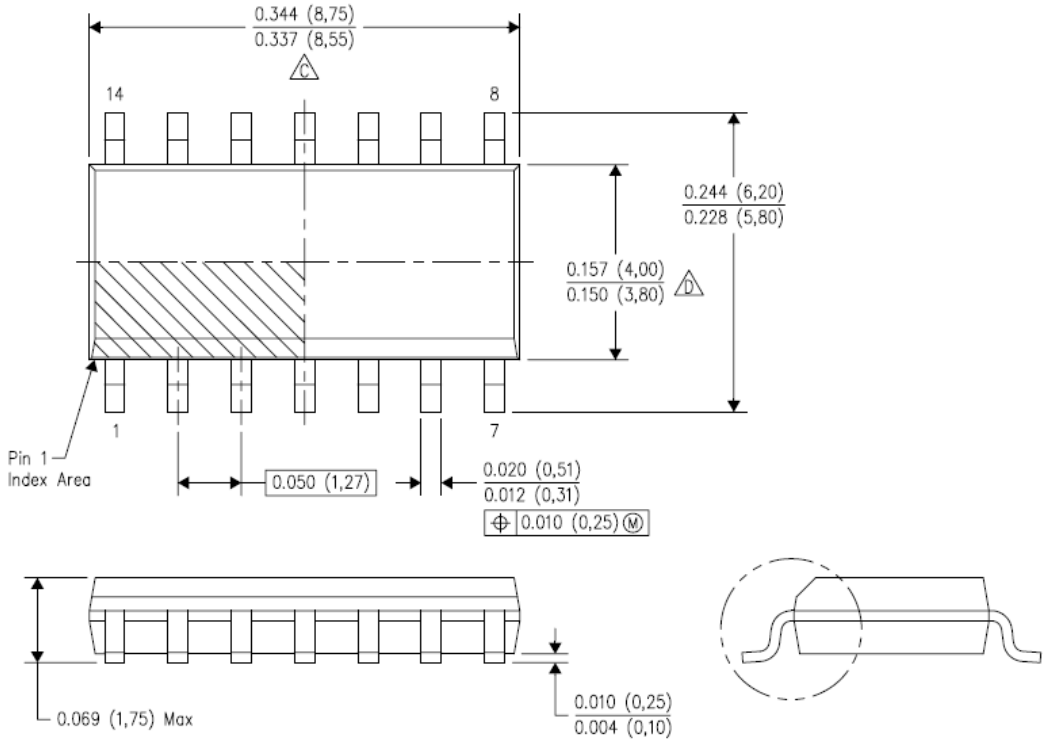
Electrical performance characteristics (Tj = +25C)

Parameter	Conditions	Min	Typ	Max	Units
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	I_C = 10μA, I_E = 0	50			V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	I_C = 100μA, I_B = 0	30			V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	I_C = 10μA, I_{CI} = 0	50			V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$)	I_E = 10μA, I_C = 0	5	6,5		V
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V, I_E = 0		0,002	5	nA
Collector Cutoff Current (I_{CEO})	V_{CE} = 10V, I_B = 0			20	nA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	V_{CE}=3V, I_C=10mA	150			
	V_{CE}=0V, I_C=1 mA	150			
	V_{CE}=3V, I_C=10μA	140			
Input Offset Current for Matched Pair Q1 and Q2 $\lvert I_{O1} - I_{IO2}\rvert$	V_{CE} = 3V, I_C = 1mA		0,02	1	uA
Base to Emitter Voltage (V_{BE})	V_{CE} = 3V, I_E = 1mA			0,75	V
	I_E = 10mA			0,8	
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2}\rvert$	V_{CE} = 3V, I_C = 1mA		0,5	1	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE3} - V_{BE4}\rvert$, $\lvert V_{BE4} - V_{BE5}\rvert$, $\lvert V_{BE5} - V_{BE3}\rvert$	V_{CE} = 3V, I_C = 1mA		0,5	1,5	mV
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	I_B =1 mA, I_C =10mA		0,1	0,15	V

Physical Dimensions in inches (millimeters)



SOIC-14 (150mil)

Revision history

Date	Revision	Changes
20-Nov-2018	**1**	Preliminary version 1